

論 文 要 旨

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<p>主論文題名</p> <p>Power Line Noise Suppression Using N-Path Notch Filter in ECG Signal Acquisition</p>			
<p>内容の要旨</p> <p>Bio-sensing activities such as electrocardiogram (ECG) and electroencephalography (EEG) are challenging to obtain high-quality electrical signals because biomedical signals have small amplitude and low frequency. When performing a biomedical signal acquisition, common-mode noise such as power line interference appears near the desired biomedical signal. It has made a problem when the power line interference has amplitude higher than the primary signal.</p> <p>Common-mode noise reduction has been recognized as important research. The driven right leg (DRL) circuit was significant and effective to suppress common-mode noise. However, in the actual ECG measurements using DRL circuit, sometimes noise still appears at the output and mismatching in the electrode impedance makes an impact to convert common-mode noise into a differential input voltage. The body in DRL circuit is expressed as a single node and cannot be used to simulate the effect of the electrode impedance mismatch. Therefore, a new body model is needed to be able to analyze the effect of electrode impedance mismatch and other problem with common body model.</p> <p>The proposed DRL circuit is an improved circuit from common DRL circuit. The first improved DRL circuit, biomedical signal is expressed by current source in parallel with electrode impedance. The simulation results of improved circuit show mismatch between right and left electrode impedance make noise appears at the output signal. The common human body from DRL circuit represented skin-electrode impedance as a single node. The second improved circuit, the skin-electrode impedance is expressed by resistance and stray capacitance are on each electrode. The simulation results of this improved circuit show the proposed circuit achieved smaller noise when stray capacitance in the arm and right leg are the same. Combination between proposed human body model and DRL circuit achieved output of the circuit is noise appear in the output signal. Therefore, human body model with DRL circuit still needs notch filter to get high-quality biomedical signals (noise-free signal).</p> <p>The other techniques to suppress common-mode noise have been proposed by using digital and analog notch filters. The technique to suppress common-mode noise used a digital notch filter, but it requires an analog front-end with a wide dynamic range since the noise contaminated input signal need to be converted to digital signal. The techniques with analog notch filter such as conventional N-path notch filters have disadvantage because these techniques require $3G\omega$ switches off-resistance and 18 paths to reach notch depth target. The problem to implement previous N-path notch filter is the difficulty in implementing switch with off-resistance. On-chip implementation of the system is also a</p>			

challenge in the realization of portable ECG devices because the notch filter has a large time constant in which requires large capacitance and high resistance.

Two topologies of N-path notch filter with leak buffer circuit have been proposed. The proposed N-path notch filters are Topology 1 and Topology 2. Topology 1 and Topology 2 achieved notch depth of 62.4dB and 63dB in measurement results with sampling frequency 50Hz, even if the proposed circuits use less number of path and small of switches off-resistance. Topology 1 and Topology 2 are verified using artificial ECG signal with 2Hz which is contaminated by power line interference with frequency 50Hz or 60Hz. Experiment results show that the proposed circuit significantly reduces the power line noise.

Topology 1 and Topology 2 N-path notch filters achieved notch depth higher than notch depth target, but have a problem in the size of capacitor. The total capacitance for Topology 1 and Topology 2 are $2.3\ \mu\text{F}$ and 930nF, respectively. Therefore, the next proposed circuit aims to propose a new technique of N-path notch filter with switched capacitance scaling to decrease the total capacitance for a fully on-chip implementation. The proposed N-path notch filter replace the resistor in N-path core into resistor equivalent of switched-capacitor to reduce the total capacitance. Topology 1 and Topology 2 with capacitor scaling and also Topology 3 using CMOS switch with total capacitance for all topologies equal to 1nF achieved notch depth higher than 40dB.

Topology 1 and Topology 2 using CMOS switch with scaling factor 1000 achieved notch depth of 64dB and 68dB, respectively. The total capacitance of Topology 1 and Topology 2 using CMOS switch with scaling factor 1000 are 2.34nF and 930pF, respectively. Below are advantage and disadvantage of Topology 1, Topology 2, and Topology 3 with/without capacitance scaling. Topology 1 with capacitor scaling is more effective in the total capacitance for on-chip implementation because of to achieve notch depth around 44dB. It used the smallest total capacitance than the other topologies.