TEMPERATURE DEPENDENT SLEEP CONTROL USING VIRTUAL GROUND VOLTAGE DETECTION FOR FINE-GRAIN POWER GATING

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ABSTRACT

Fine-Grain Power Gating (FGPG) is a technique in which a high-Vth transistor (Power Switch) is inserted between low-Vth logic circuit and the ground to reduce leakage in the idle state. This paper describes a sleep control technique using leakage monitor circuit to implement FGPG. This technique controls Power Switch (PS) by a signal wire that is charged by leakage current. Since the sleep control circuit can be made small, energy overhead due to the sleep control circuit becomes smaller in comparison with the conventional methods. Furthermore, at high temperature, the leakage monitor quickly turns off the PSs. In contrast, at low temperature, the leakage monitor slowly turns off the PSs. For this reason, the technique enables us to realize efficient run-time power gating depending on the temperature. We evaluated leakage energy dissipation by using simulation for a microprocessor which applied FGPG. We ran DCT, Qsort and JPEG programs at the simulation. The impact of circuit conditions is also discussed. Using our method, the total leakage energy decreased to 13% as compared to non-power-gating at the maximum and the energy share of the control circuit was reduced to 2%.

1. INTRODUCTION

With the spread of portable devices, reducing energy dissipation of LSI has become one of the most critical requirements. In particular, leakage current is an important subject of low power LSI when we use miniaturized transistors [1].

Power Gating (PG) is a well-known technique in which a high-Vth transistor (Power Switch) is inserted between low-Vth logic circuit and the ground to reduce leakage in the sleep state. We can classify the technique as coarse grain and fine grain power gating. Coarse-Grain Power Gating (CGPG) has been applied to commercial microprocessors [2]. By contrast, Fine-Grain Power Gating (FGPG) is an approach to apply PG in finer granularity to and increase opportunities for PG [3, 4]. This technique can reduce more leakage energy because it can reduce leakage current at fine intervals. However, in FGPG, energy overhead due to turning on and off PS becomes serious. This is because the time when a circuit is idle state is the nano (n) second order in FGPG whereas the time is the micro (μ) second order in CGPG. It is necessary for PG control to consider the Break Even Time (BET) in FGPG. BET is minimum idle time to get energy savings. This is because power switch (PS) incurs switching energy as the energy overhead. Ideally, PG should be enabled only at idle events whose idle time is longer than BET. However, it is difficult to determine whether the idle cycles exceed BET when a circuit enters the idle state. Several sleep policies to deal with this problem have been proposed. However, any of those techniques did not consider energy overhead by control circuits for PG.

We present a new sleep policy called “Charge-up Delay (CuD)” policy to implement FGPG [5]. This policy controls a PG circuit by monitoring the voltage of Virtual Ground (VGND) voltage that is raised by leakage current. In this paper, we demonstrate leakage energy dissipation and circuit area by using simulation for a microprocessor which applied FGPG.

2. FINE-GRAIN POWER GATING

FGPG has emerged as a technique to power gate the internal logic blocks of a processor in a fine-grained manner while running the entire processor [4]. The paper [4] presents the CPU which applied FGPG to four internal function units (FUs) such as ALU, shifter (SHIFT), multiplier (MULT) and divider (DIV) in 65nm CMOS technology. The method of sleep control for FGPG is shown Fig.1. A standard pipeline structure consists of Instruction Fetch (IF), Instruction Decode (ID), Execution (EX), Memory Access (MEM), and Write Back (WB) stages. Additionally, FUs which applied PG independently is controlled by a sleep controller. In IF stage, the sleep controller judges which

FU is to be used. Hence FUs can be powered off in a fine-grained manner while running the entire processor. Because run-time FGPG increases opportunities for PG, it can reduce more leakage energy as compared with CGPG. However, since the powered-off period is short in FGPG, energy dissipated at the power-off and power-on becomes a critical overhead in energy saving as shown in Fig.2. Therefore, we need to consider the minimum idle time to get energy savings. BET is a time at which the energy reduction by PG is equal to the total energy overhead.

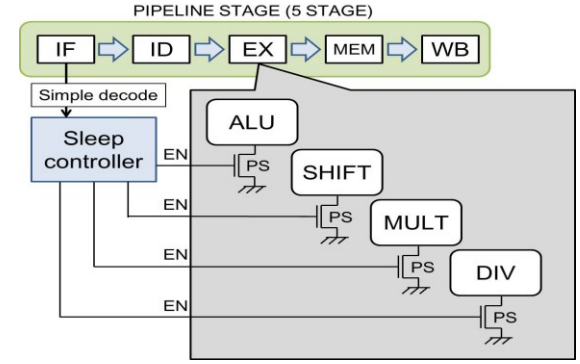


Fig. 1 Sleep control for FGPG.

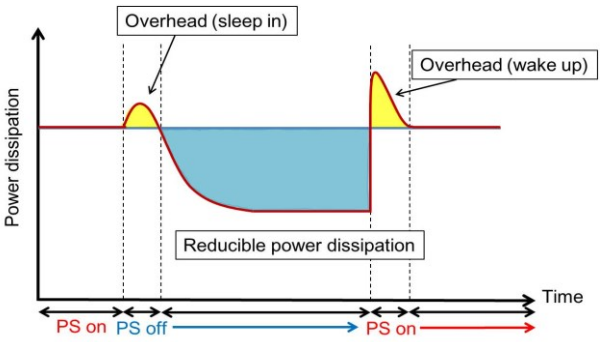


Fig. 2 Overhead for FGPG.

3. CONVENTIONAL SLEEP POLICIES

3.1 Whenever Idle Put to Sleep policy (WIPS).

In WIPS policy, a circuit is powered off as soon as it becomes idle states. It is very easy to implement but energy dissipation may not be reduced (or even increase) when idle events whose idle cycles are shorter than BET occur frequently.

3.2 Time-Based policy (TB).

The paper [3] proposes the sleep policy for FGPG called TB policy. As shown in Fig.3, the TB policy starts counting idle cycles when the idle state is detected and PG is enabled when the counted cycles (i.e. idle time) reach BET. This policy reduces the possibilities that PG is enabled (i.e. PS is turned off) for the idle cycles shorter than BET. However, a register to store the BET value and a comparator to compare the counted value and BET are required. Since the counter and the comparator consume dynamic power at each cycle, this becomes energy overhead of the control circuits. Furthermore, TB policy in which clock gating and clock division are applied to the control circuit reduces control energy dissipation.

An adaptive TB policy (ATB) in which the temperature dependence of BET is considered and the TB policy is applied based on BET at the detected temperature has been proposed in [6]. The authors of [6] proposed an on-chip detection methodology for BET by using a monitor circuit. This policy allows us to reduce more leakage energy than the TB policy. However, this requires not only a circuit to monitor temperature-dependent leakage current but also a Look-Up-Table (LUT) to convert the leakage monitor output to BET in the control circuit.

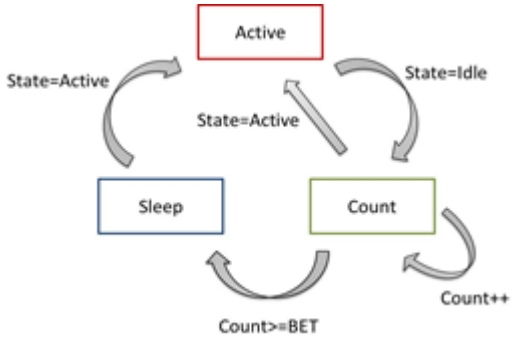


Fig. 3 TB policy control sequence.

4. PROPOSED POLICY: CHARGE UP DELAY POLICY (CUD)

We propose a novel sleep policy named “Charge –up Delay (CuD)” policy in which an on-chip leakage monitor directly controls the turn-off timing of a power switch of FU. Fig.4 depicts the structure to realize the CuD policy. The major components are a sleep controller and a leakage monitor. When FU becomes idle, the sleep controller directs the leakage monitor to begin leakage-monitoring by changing the enable signal from 1 to 0. Depending on the amount of leakage current, the transition time of the leakage-monitor’s output “OUT” from 1 to 0 varies. For less leakage, the transition time of OUT becomes longer and thereby the turn-off timing of PS is delayed. Inversely, for more leakage, the transition time of OUT gets shorter and thereby PS is turned off earlier. Thus, the turn-off timing of PS is controlled depending on the amount of leakage current. In the following sub-sections, we describe circuit structure of the leakage monitor and the control scheme more in detail.

4.1 Leakage monitor circuit

Fig.5 shows the circuit structure of leakage monitor. The leakage monitor is composed by a leak generator and a voltage comparator. When EN signal becomes ‘0’, the signal line of VGND is charged up slowly by a subthreshold leakage current flowing through a pMOS transistor in the leak generator. The voltage level of VGND is compared with VREF in the voltage comparator. When the voltage of VGND exceeds VREF, the signal OUT transitions to 1. The VREF voltage was set to 0.5V for the supply voltage VDD of 1.2V.

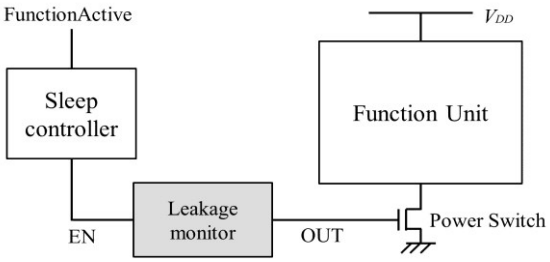


Fig. 4 Hardware organization of CuD policy.

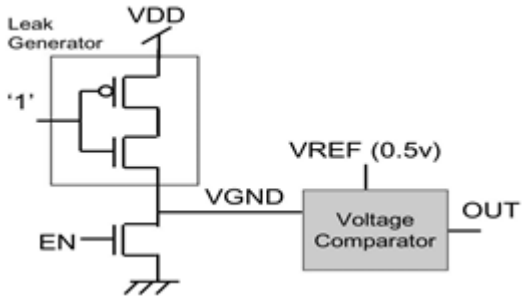


Fig. 5 Circuit structure of leakage monitor.

5. EVALUATION

5.1 Setup for energy estimation

We performed evaluation with a MIPS R3000 based CPU chip in which FGPG was applied to FUs. The chip was implemented in 65nm technology. Fig. 6 shows the share of leakage power in the entire CPU. The result does not include the cache power. FUs occupy 60% of the total leakage power. The leakage power is not only dissipated at active time but also at idle time. In this paper, we investigated the reduction of leakage energy dissipation of FUs by run-time PG. In order to analyze the energy dissipation of each FU during the idle period, we performed the circuit level simulation using a Hsim. We also performed the Verilog simulation of the RTL model for evaluation of sleep policies and analyzed the energy dissipation of the control circuit. As application programs for the CPU, we ran DCT, Qsort and JPEG programs at the simulation. We calculated leakage energy dissipation for each program using idle events and the energy dissipation of each idle time in the sleep policies as shown Fig. 7.

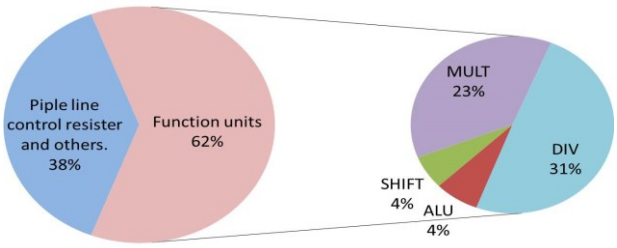


Fig. 6 The share of leakage power in a MIPS R3000 based CPU.

Each program for sleep policies

Idle cycle	Number of events
1	240
2	384
4	96
12	48
25	48
33	48
38	48
40	84
81	48
82	48
82	96
200	150

Energy dissipation of FU at each idle cycle

Idle cycle	Energy dissipation(pJ)
1	0.9
2	1
4	1
12	1.4
25	1.7
33	1.9
38	2
40	2
81	2.9
82	2.9
82	3
200	4.4

Energy dissipation of FU for programs

Fig. 7 The calculation method at each program.

5.2 Energy dissipation evaluation at each program

Fig. 8 shows leakage energy dissipation of four FUs of the CPU and control circuits with sleep policies for DCT, Qsort and JPEG. Energy value is normalized by that of Non PG. The CPU is designed in 65nm CMOS technology at supply voltage of 1.2V. Additionally, energy dissipation of control circuit is energy which is required to implement the each PG policy. VREF for CuD policy is supplied at 0.5V. At 25°C, TB and ATB policies perform the same PG control to FU. However, at high temperature, ATB policy detects temperature and controls FU in consideration of the temperature dependence of BET. Energy dissipation of temperature monitor and LUT are not considered. This is because the temperature monitor and LUT operate infrequently and hence their energy dissipation can be ignored.

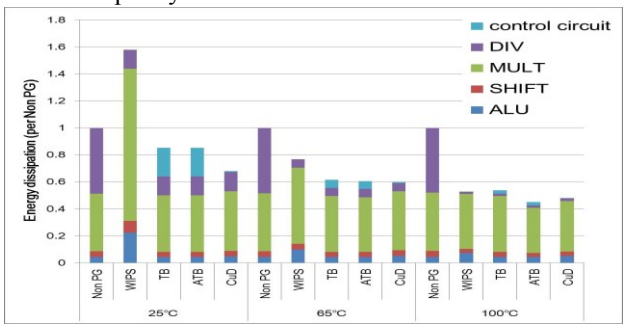
In ALU, the long sleep does not exist irrespectively of the temperature or application programs. From this observation, the best way to get gain in energy savings is to always disable PG in ALU. The CuD policy is the second best. This is because the CuD policy always disables PG also. The ATB policy does the PG control similar to CuD policy. However the CuD policy reduces the energy dissipation for control circuit. In WIPS policy, at ALU, the leakage energy dissipation increase to 4x as compared to Non PG.

On the contrary, the DIV is inactive for almost all the time because it is rarely used. Hence the WIPS policy achieved the smallest leakage energy dissipation among the sleep policies at every temperature and program at DIV. The WIPS policy decreases energy dissipation to 31% as compared to Non PG in Qsort at 25°C. However, the energy dissipation of control circuit was large for TB and ATB policies. Since energy dissipation in the control circuits is almost neglected in the CuD policy, the CuD policy achieved smaller total energy dissipation in DIV as compared to ATB policies irrespectively of the temperature or application.

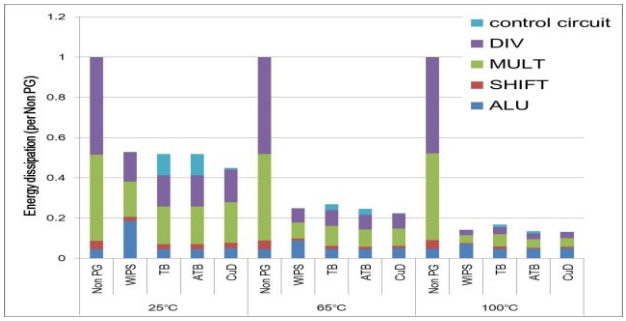
For the SHIFT and the MULT, the ATB policy archives the smallest leakage energy dissipation of FUs for each program. However, for the ATB policy, the energy dissipation of control circuit is large at 25°C and 65°C. Hence energy dissipation including control circuit is smallest at CuD policy as compared to the ATB policy.

In total energy dissipation including leakage energy for FU and control energy, the CuD policy achieves the smallest energy dissipation at 25°C and 65°C for each program. This is because the CuD policy reduces the

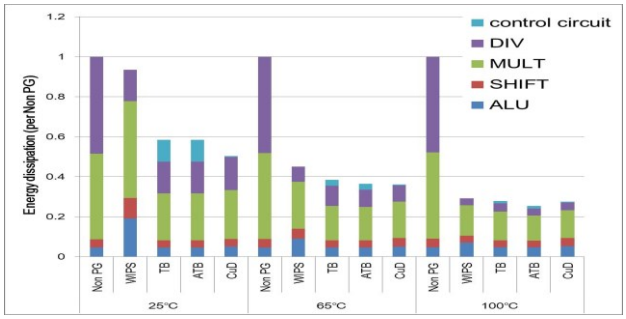
possibilities to power-off at short sleep and the energy dissipation of control circuit for this sleep policy to 2%. In contrast, at 100°C the ATB policy achieved the smallest total energy dissipation and the CuD policy does the second best. This results show that the CuD policy is able to achieve the small total energy at irrespectively of the temperature or application. the total energy dissipation reduced to 69% at 25°C, 60% at 65°C and 48% at 100°C. Additionally, the energy dissipation decreased to 45-13% for Qsort and to 50-37% for JPEG with CuD policy.



(a) DCT program



(b) Qsort program



(c) JPEG program

Fig. 8 The energy dissipation for sleep policies.

CONCLUSION

We proposed a new sleep policy using a leakage monitor circuit and presented the evaluation results of the sleep policies application programs. The simulation results demonstrated that our proposed policy effectively reduces the energy dissipation of the control circuit and leads to more energy reduction than the conventional sleep policies. Using our policy, the total leakage energy decreased to 13% at the maximum and the energy share of the control circuit was reduced to 2%.

REFERENCES

[1]W. Hu et al., "Godson-3b1500: A 32nm 1.35GHz 40W 172.8Gflops 8-core processor," ISSCC'13, pp. 54-55, 2013.

[2] R. Kumar and G. Hinton, "A family of 45nm IA processors," ISSCC'09, pp. 58-59, 2009.

[3] Z. Hu et al., "Microarchitectural techniques for power gating of execution units," ISLPED'04, pp. 32-37, 2004.

[4] N. Seki et al., "A fine grain dynamic sleep control scheme in MIPS r3000," ICCD, pp. 612-617, 2008.

[5] M. Kudo, K. Usami, "Sleep Control Using Detection of Virtual Ground Voltage for Fine-Grain Power Gating", ITC-CSCC'13, pp.392-395, Jul. 2013

[6] K.Usami et al., "On-chip Detection Methodology for Break-Even Time of Power Gated Function Units," ISLPED'11, pp241-246, Aug. 2011

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